# PVT Analysis and Behavioral Modeling of Doherty and Envelope Tracking RF ULP Power Amplifiers using 65 nm CMOS Technology

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#### Abstract

This research encompasses both Process-Voltage-Temperature (PVT) considerations and behavioral modeling of two proposed Power Amplifier (PA) designs for wireless communication systems. Process variations, supply voltage changes, and temperature changes provide difficulties for the design and optimization of power amplifiers for wireless communication systems and may have a substantial influence on their effectiveness. PVT analysis and behavioral modeling have been conducted to address the aforementioned challenges and characterize the behavior and performance of the power amplifiers under real-world operating conditions. It investigates the impact of process variations, supply voltage variations, and temperature variations on the performance of the PAs. The insights gained from this analysis contribute to a deeper understanding of the power amplifiers' performance, efficiency, and suitability for specific wireless communication standards, laying the foundation for future advancements in RF power amplifier design. The first design focuses on a Doherty PA (DPA) tailored for lowpower short-range applications complying with the IEEE Wireless Personal Area Network (WPAN) standard. The second design explores an Envelope Tracking (ET) supply bias control for low-power long-range applications conforming to the IEEE Wireless Local Area Network (WLAN) standard. By examining these factors, the research ensures that the PAs exhibit reliable and optimal performance under real-world operating conditions. The PVT corners show a change in gain of only 0.4 dB for DPA and 0.9 dB for ET PA. Furthermore, behavioral modeling is employed to characterize the power efficiency of the envelope tracking PA, along with the current efficiency and quotient current on the load current scale. These models provide valuable insights into the behavior and performance of the PAs at a higher level of abstraction. The results and findings contribute to a deeper understanding of the PA's performance, efficiency, and suitability for specific wireless communication standards, laying the foundation for future advancements in RF power amplifier design.

Index Terms: Behavioral Modeling, CMOS Technology, Power-Added Efficiency, Process-Voltage-Temperature, Radio Frequency.

#### I. INTRODUCTION

In the present world, where people use more healthcare, smart workplaces, smart homes, the web, social media, and utility applications, everyone demands less time to recharge their portable devices [1].

Wireless technologies that are low-cost, power-efficient, linear, and have a small form-factor have been in high demand since the last decade. These days, having a battery that has a long life expectancy is a critical and essential need. In addition, the challenge in current wireless communication systems is to provide high data rates in advanced modulated RF signals with a narrow-band and Ultra-Low Power (ULP) utilization.

IoT-driven devices are predicted to reach a market worth of more than \$75 billion in 2025, up from a market of over \$15 billion in 2015. Over the ensuing ten years, this number is expected to increase rapidly.

Figure I estimates a huge number of IoT-connected devices worldwide (in billions) from 2015 to 2025 [2]. As the IoT becomes a reality, the rate of change in the semiconductor market will accelerate significantly. Currently, a

tremendous volume of data is sent across short and long distances using mobile communication networks like Bluetooth connections, wireless LAN, cell phone internet protocols, and interactive media offerings including video games, movie streaming, music downloads, and cloud services. These communication systems need massive data rates and sufficient power to be handled.

In order to handle this enormous growth and boost bandwidth efficiency, more complex modulated signals like OFDM, QAM, and QPSK have been used at present, and probably in future generations of wireless systems.

As a consequence, extensive research on PA design is still being conducted in both academia and industry, leading to several advancements in methods for maintaining efficiency dominating low power.

The PA design has advanced significantly during the last decade, relying on very complicated transmitter topologies to address linearity and efficiency trade-offs [3].





Figure I: Expected IoT-Connected Devices Worldwide (in Billion) from 2015 to 2025

### II. ULP CMOS RF POWER AMPLIFIERS FOR LOW POWER IEEE STANDARDS

The Power Amplifier (PA) is the most power-hungry component of the RF transceiver, portraying design issues. These include insufficient connectivity, power distribution, bandwidth, linearity, and efficiencv parameters that did not match system requirements. The primary challenge in a PA design is achieving higher efficiency while maintaining linearity over bandwidth with a wide range of output power levels [4]. The Power-Added Efficiency (PAE) is a Figure-of-Merit (FoM) that indicates how well the PA transforms DC power to RF power. Designers have raised concerns about PA in the front end of wireless radios because of the system's significant power consumption. There has been a lot of study on PA methods for optimizing PA efficiency [5]. It is a challenging measure in the design of PAs for various lowpower IEEE 802 wireless standards. The result of this study's primary concern and problem is this issue, which presents the design and optimization of two Ultra-Low Power (ULP) PA architectures using 65nm CMOS technology. Figure II graphically interprets the theory behind power efficiency by defining the concept of transmitted power over dissipated power. The power dissipated is at load, obviously, which exhibits or revels in the form of heat. Particularly, a linear PA using OFDM and a constant voltage supplied yields a 20% efficiency [6].

#### A. ULP DPA with Fixed Inter-Stage Capacitances for Short-Range and Low Power IEEE 802.15.4 WPAN Standard

Study [7] presented a ULP Doherty PA (DPA) architecture with fixed inter-stage capacitances. The main amplifier and the peaking amplifier have been designed and optimized with power divider & combiner models using equivalent lumped parameters. Due to 40 MHz narrowband communication (2.4 - 2.44 GHz ISM band), it offers fixed capacitances before the input-impedance stages, for a perfect impedance matching at both stages. The novel design shows 2.1 mW ultra-low DC power consumption, 29.2% PAE, and 4 dBm P1-dB compression point. The post-layout simulations show an extremely high gain of 10.14 dB, very low input-insertion loss of -11.9 dB, and very strong drive current capability of 547  $\mu$ A & 663  $\mu$ A for main & peaking PAs respectively. Impedance matching is acquired to achieve the desired harmonic suppression at the output of the DPA design. the consequences are all in comparison to state-of-the-art PA architectures for ZigBee and similar devices under shortrange and low-power IEEE 802.15.4 WPAN standards.

The main and peaking amplifiers are often pre-matched using a free scale. These two amplifiers perform the operation with a 900-phase difference. This is accomplished with a Wilkinson power divider or a hybrid splitter with a 900-phase shift. At the main amplifier's output, a 900 transmission line is used to accomplish this division. When the main amplifier's input signal level rises to its saturation level, the peaking PA begins to create power, nevertheless, on the other side, this phenomenon is referred to as the impact of load modulation since it also causes the main amplifier's output impedance to rise [8]. The analogue BPSK has a modulation index of 0.5 which offers an output power of 0dBm (1 mW) for around 10m range. The power combiner ideal model operates at a 2.4 GHz band with two output ports dividing the power equally. This is because inductive splitters, cause a 90° phase shift between the two signals. Both the peaking amplifier and the main amplifier are intended to be loaded at Z0 Transmission line input impedance has been calculated using both equal and unequal power divider approaches in a number of older designs. The  $\lambda/4$ transmission line equals  $\lambda/4 = \sqrt{2}$  Zo= $\sqrt{2}$  (100) = 70.71 $\Omega$  for this scenario, where a complete match of  $50\Omega$  is needed. To improve the power-added efficiency (PAE), C1 and C2 are added as fixed interstage capacitances. The divided impedance is Z1 and Z2, which is recombined with the power dissipation to get the perfect matching throughout the PA stages. Pi-network does the 900 phase shift at one of the ports. Figure II illustrates the proposed schematic of proposed DPA using 65 nm CMOS technology, which has been transformed into a functional diagram.



Figure II: Functional Block Diagram for Proposed ULP DPA using 65nm CMOS Technology

#### B. ET Supply Bias with Cascoded Cells Terminated as Class-F ULP-PA for Long-Range and Low Power IEEE 802.11ah WLAN Standard

Study [9] presented a Class-F architecture with ET supply bias to increase the efficiency of overall PA design. The ET consists of a pre-amplifier before the Envelope Detector (ED) in a cascaded linear model, to increase efficiency and reduce DC power consumption. The gateto-drain feedback in the PA's two cascoded cells, terminated as Class-F, helps to improve linearity and reduce harmonic content in the input signal. The novel design meets the requirements of the IEEE 802.11ah standard for long-range low-power WLAN by using a DC power consumption of 3.75 mW, a PAE of 37.1%, and an operating frequency in the unlicensed 915-931 MHz band in the United States. The chip layout size is reduced to just 0.13mm<sup>2</sup> by the ET inductor-less supply bias design.

The preamplifier is connected prior to the envelope detector for voltage amplification and tracking. The proposed schematic is an inductor-less design that saves up to 45% more area than ULPA DPA. No inductor has been used and even the matching at the RF input is done using a pure capacitive network. The preamp consists of two MOS with Common-Source (CS) and Common-Drain (CD) stages. CD low impedance at the output is an excellent fit for the next stage as this buffer mainly acts as a matching circuit for the next stage. The capacitive matching network with the RF input maintains the narrowband matching and occupies less area as compared to the LC matching network which exhibits a lot of space. A Class-F configuration consisting of two-cascoded cells that are actually terminated as Class-F. For a standard configuration, each transistor consists of a Common-Gate (CG) with a fixed-bias gate-voltage and a Common-Source (CS) as a trans-conductance stage. The CG stage is prevented from entering the triode region at a high output power region by the corresponding RF AC signal to the gate node of the CG stage. The parasitic gate-drain capacitance maintains a constant level in this regard, enhancing linearity. Figure III illustrates the functional block diagram for the proposed ULP ET PA with twocascoded cells terminated as Class-F and using 65nm CMOS technology.



Figure III: Functional Block Diagram for Proposed ULP ET PA with Two-Cascoded Cells Terminated as Class-F and using 65nm CMOS Technology

## C. Layout Schematic of the Proposed ULP RF PA using 65nm CMOS Technology

The design flow's last simulation phase was transforming the schematic design into a layout. The analytical process is quickly entered using ADE-L, and simulations are conducted. The chip layout features a 0.29 mm<sup>2</sup> active area [10]. The power-rails are used instead of the pads and the pad-effect is included. The ADE-L tier capabilities are expanded by ADE-XL, which offers multiple test support, analysis across sweeps and corners, direct access to all findings, and the ability to generate comparison sheets and datasheets as necessary. Appropriate metal layers were chosen to ensure proper signal propagation and minimize losses. The Design Rule Check (DRC) of 0.47 for TSMC 65nm CMOS technology was kept in mind before placing lines. During the construction process, vias and contacts were strategically placed to establish connections between different metal layers and between the micro-strip lines and active device layers. This facilitated the integration of the micro-strip lines into the overall circuit layout and ensured proper signal flow. Very few orthogonal lines are visible on the layout. However, the 45-degree lines and bend curves are largely preferred. Figure IV represents the layout schematic of the proposed ULP DPA and ULP ET PA using 65nm CMOS technology. Table I summarizes the comparison of the performance of state-of-the-art ULP RF PA design trends in recent years.





Figure IV: Layout of Silicon Footprint Showing 45% Reduction for ET PA reported in [7] and [9]; (a) Layout of ULP DPA (0.29 mm<sup>2</sup> Silicon Layout Footprint), (b) Layout of ULP ET PA (0.13 mm<sup>2</sup> Silicon Layout Footprint)

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Specification	ULP DPA	ULP ET PA
Technology	65 nm	65 nm
Year	2022	2021
IEEE Standard	802.11 ah	802.15.4
Frequency	Sub-1 GHz (915 MHz)	2.4 GHz
Supply Voltages	1.2 V	1.2 V
ULP/ LP	ULP	ULP
DC Power Consumption	3.75 mW	2.1 mW

Output Power	14dBm with Saturated Output Power of 22 dBm	1.65 dBm
P1-dB Compression Point	14.3 dBm	4.0 dBm
Input Return Loss (S11)	-15.05 dB	-11.9 dB
Gain	11.86 dB	10.14 dB

#### III. PVT CORNER ANALYSIS AND BEHAVIORAL MODELING

This research builds on the author's earlier work, which involves the rigorous design and assessment of proposed PAs and seeks to further understand how they operate by analyzing how they react to various process, voltage, and temperature conditions. The research aims to shed light on important parameters such as power efficiency, current efficiency, and quotient current on the load current scale by performing PVT analysis and creating behavioral models, thereby providing helpful insights into the behavior and performance of the PAs in real-world operating scenarios. Using the information and experience gathered from the functional block-sets, this section describes the approach used for the PVT analysis and behavioral modeling.

### A. Process-Voltage-Temperature (PVT) Variations for Simulation Results

The choice of PVT corners for a CMOS RF PA design depends on several factors, including the technology node, the specific design requirements, and the expected operating conditions. The study [11] shows some general guidelines for choosing PVT corners for CMOS technology. The process is marked slow (SS) for the design which requires low power consumption, voltage to typical as the design needs to operate under low-power supply conditions, and the temperature to typical as the design is intended to be used in temperature-controlled or room temperature environment. The analogue design environment launches the global voltage variable 'VDD' with 1.2 volts which is further varied. The corner setup adds corners from two typical corners which are used to verify the performance of PA designs. The two convention letters of corners (C0 and C1) represent are performance of n-MOS. Since there is no p-MOS used, so selecting the fast (FF) variable shows no means. The aforementioned process controls are selected on Process-Development-Kit (PDK) model file for analysis. The process chosen SS (slow) at C0 defines the process as less than the typical threshold or subthreshold regions [12]. Additionally, the process of NN (nominal) at C1 is considered as an alternative process-variation test. NN shows the nominal or ideal bench test. The voltage variations are assumed with 10 percent tolerance showing the ranges: 1.188 to 1.212 volts. These ranges are similar to all two corners and a set as 1.188, 1.2, 1.212. Temperature ranges are assumed to be from 0 to 45 degrees (0, 25,45). The voltages and temperature [13] values are placed in both corners C0 and C1. Figure V (a) and figure V (b) show the gain variation of DPA and ET PA with the change in temperature on the aforementioned range respectively. As observed the

change in gain is only 0.4 dB for DPA and 0.9 dB for ET PA.



(b)

Figure V: The Gain Variation of DPA and ET PA with the Change in Temperature during PVT Analysis; (a) The Gain Variation of DPA with Temperature, (b) The Gain Variation of ET PA with Temperature

#### B. Response to the Adaptive Bias Approach for Drain Current and Drain Voltage Behavior for ULP DPA

Although the response to the biasing approach looks not as ideal as expected in the classical DPA simulation method. The magnitude of the fundamental current and voltage for the main device and the peaking device in response to rising input voltage is shown in figure VI. We can see that the main voltage climbs linearly until it hits saturation in the low power zone below the transition or threshold point (~0.4 V) [14], while the main current likewise increases linearly, as predicted by theory, to reach a current of over 600µA. The high-power zone starts at the transition point voltage, and the fundamental current given by the peaking device increases from zero to practically the same maximum current as the primary device (or a little more than the main device's current i.e., ~>600 µA), while the voltage stays mostly linear. Keep in mind that some expansion is seen as a result of the main amplifier's compression as the input voltage rises and the device's lessthan-ideal behavior. The inputs provided to the CAD tool are generally preferred to be chosen as Pin. The similar input voltage ranges, from -20 dBm to -7 dBm which are in synchronization to PAE highest achieved values on preand post-layout simulations [15], are contrasted to input voltages for the statistical results of drain current and voltages, for the main device and the peaking device respectively.



Figure VI: Response of the Adaptive Bias Approach

#### C. Power and Efficiency of ET PA using MATLAB as Behavioural Modeling

Working with probability distributions is a key aspect of using statistics for data in simulation software includes three GUIs as well as command-line tools that make it easy to look at probability distributions [16], generate random samples from them, or fit them to your data will discuss two of the GUI's briefly and then discuss the distribution fitting tool in more detail. The first GUI will introduce let us look at probability distributions and determine how their parameters affect their shape to open this GUI type of distribution tool at the simulation software command prompt. This GUI lets us select which of the twenty available distributions we want to look at and whether you'd like to view the probability density function or cumulative distribution function for the distributed data. We will look at the PDF for our normal distribution you can change the mean and standard deviation for the distribution and see how its shape changes. This GUI is excellent for developing an intuitive understanding of probability distributions. The second GUI will introduce and generate random samples from any of the twenty available probability distributions and display the samples as histograms (or any other graph plot preferred). It also allows to export, the random samples for the workspace which one can use to test hypotheses or models under different conditions to open this GUI type of "Random" tool at the simulation software's command prompt. First, we create '1' as the mean and '2' as the standard deviation to characterize a normal distribution and generate a random sample from it. The GUI creates and displays this sample in about a second. We click the resample button to generate another random sample and export the sample to the workspace. A cure-fitting tool at the command prompt, the distribution fitting tool lets you fit predefined probability distributions or your own custom distribution to your data set. It makes it easy to pre-process your data set visually analyze fit quality compare multiple fits and evaluate fit results the distribution fitting tool has several task buttons for creating analyzing and managing the distributions.

Getting the most out of the system is one of the key goals of the planned ET PA. When choosing an operating point and input/output parameters during the optimization process, an accurate power loss model is particularly helpful. Modern research publications use a variety of power loss models, including:

- Physics Modelling
- Behavioral Modelling
- Analytical Modelling

Physics-based models often contain a high degree of detail, which leads to computations that take a lengthy time in addition to being very accurate. The accuracy and calculation time of the behavioral model must be balanced, however, without taking into account the static and dynamic nonlinear effects, accuracy issues may arise. The analytical model can provide simulations reasonably quickly and contain equations that account for the converter's non-ideal behavior. A hybrid model that combines both the behavioral analytic loss model and the suggested PA's efficiency optimization is described in [17].

This paradigm offers several benefits, which may be summed up as follows:

- The model has decent ULP range accuracy (lower than 10 mW) [18].
- Due to their high-frequency operation, n-MOS and p-MOS parasitic inductances are taken into consideration.

Analytical procedures include the nonlinear forward transconductance and nonlinear parasitic capacitances. The model's specifications for 65 nm CMOS technology may be found in the datasheets. It should be underlined that the model of nonlinear capacitors and changing transconductance is crucial for preventing significant estimate errors in efficiency. With different equivalent circuits for each sub-period of transition, distinct state variables for each period, iterative numerical calculation of the state variables evolution with a fixed time-step, and consideration of the energy stored in the parasitic component, it can be concluded that the main approach is this. The model separately analyses the high side turn-on and high side turn-off between high and low PAPR levels as the two primary transitional phases. Similar to previous tools, starting with the steady-state circumstances at the start of the transitions, it is possible to determine the principal waveform and the losses. A purposefully clipped OFDM signal or an OFDM signal that operates in an amplifier's saturation region were both taken into account by [19]. Be aware that depending on the saturation level. these types of warped OFDM signals produce an error floor. The research looked at the PD of M-QAMmodulated OFDM signals [20]. Theoretically, the continuous Gaussian PD of the mth OFDM symbol with 'N' subcarriers is not present, and the PD is a function of 'm', where 'm'  $\in [0,1..., N-1]$ . Additionally, it deduced the PD for illustrative situations of  $m \in [N/4, 2N/4, and 3N/4]$ . It presented a generic form of the PD for,  $m \in [0, N/4,$ 2N/4, 3N/4]. Figure VII plots the simulation software tool results, where the linear power losses and the linear ET PA's efficiency are modelled.

The efficiency of the ET PA is computed with the power loss of linear cascaded PA:

$$P_{converter} = \int P_{dist.}(v_{out}(t)) \cdot P(I_{out}, v_{out}) dv_{out}(t) \quad (1)$$

$$P_{converter} = \int P_{dist.}(v_{out}(t)) \cdot P(I_{out}, v_{out}) dv_{out}(t) \quad (1)$$

$$P_{linear} = \frac{\int v_{out}(t)(v_{out}(t) - v_{in}(t)).dt}{R_L}$$
(2)

Where:

 $P_{dist.}$  is the probability distribution of envelope waveform v<sub>out</sub>(t), and P<sub>converter</sub> is the function observed as output voltage and current as seen from input to output stage.

The simulation time for an envelope with a bandwidth of 16 MHz is greatly reduced by this probability distributionbased technique for power-loss conversion.  $P_{linear}$  can be found using the original envelope and the full slow envelope if the overall resistance of the load (main PA) is known.



Figure VII: Power Losses Behavior Resulting from Linear Amplifier Simulation Software's Stagnant (Slower) Envelope

#### IV. RESULTS AND DISCUSSION

The study presents the design and implementation of two Ultra-Low Power (ULP) CMOS Power Amplifier (PA) solutions targeting Internet-of-Things (IoT) applications. The first PA operates at 915 MHz based on the 802.11 ah standard and is implemented in 65nm CMOS technology with a 1.2 V supply voltage. It achieves 14 dBm output power with 37.1% peak power added efficiency (PAE) and 11.86 dB gain while consuming only 3.75 mW DC power. The PA employs a Class-F topology along with an Envelope Tracking (ET) supply-bias feedback technique to improve efficiency. Compared to prior state-of-the-art designs, this PA demonstrates the highest PAE reported to date for a sub-1 GHz ULP PA in 65 nm CMOS, while achieving one of the lowest power consumption levels. The second PA is an ultra-low power differential PA designed for 2.4 GHz operation based on the 802.15.4 standard, also implemented in 65 nm CMOS but with a 1.2 V supply. It achieves 1.95 dBm output power, 29.85% peak PAE, and 10.33 dB gain while consuming just 2.14 mW DC power pre-layout and 2.10 mW post-layout. This PA uses a fixed inter-stage capacitive divider topology optimized for 40 MHz narrowband operation. Compared to prior arts, it demonstrates comparable PAE but significantly lower power consumption while operating at a lower supply voltage. In summary, the two presented PAs achieve excellent PAE performance through advanced circuit techniques like Class-F, ET supply modulation, and

capacitive divider-based differential topology. More importantly, they accomplish this while operating at very low power levels suitable for energy-constrained IoT edge devices. The ultra-low power consumption of just a few mW while still achieving high efficiency in the 30% range and moderate output power in the 1-14 dBm range makes these PAs suitable for battery-limited IoT applications. The low supply voltages of 1.2 V also play a key role in enabling the ULP operation. Compared to state-of-the-art prior CMOS PAs, these designs push the envelope of achieving higher efficiency at lower DC power levels, paving the way for more energy-efficient wireless connectivity in emerging IoT use cases. The techniques presented to optimize PAE while minimizing power can be extended to design ULP radios for other sub-GHz and 2.4 GHz standards like Bluetooth, ZigBee, Thread, and Wi-Fi. Overall, the PAs demonstrate outstanding power efficiency critical for IoT edge devices while delivering sufficient output power for short-range wireless links.

This research thoroughly covered the Process-Voltage-Temperature (PVT) concerns and behavioral modelling elements for two suggested Power Amplifier (PA) designs designed for wireless communication systems. A DPA that adhered to the IEEE Wireless Personal Area Network (WPAN) standard and was optimized for low-power, short-range applications was the focal point of the initial design. In the second design, the IEEE Wireless Local Area Network (WLAN) standard's ET supply bias control was investigated for use in low-power, long-range applications. The effects of process changes, supply voltage fluctuations, and temperature variations on the performance of the PAs were thoroughly examined by the PVT study. This extensive testing made sure that the PAs delivered dependable and ideal performance under actual operational circumstances. With just a 0.4 dB variance for the DPA and a 0.9 dB variation for the ET PA, the findings of the PVT study confirmed the resilience of the designs. Additionally, behavioral modelling was crucial in characterizing the envelope monitoring PA's power efficiency and evaluating the current efficiency and quotient current on the load current scale. These models were used to gain important insights into the behavior and functionality of the PAs at a higher level of abstraction, allowing for a greater comprehension of their functionality, effectiveness, and compatibility for certain wireless communication protocols. By establishing an excellent foundation to support further improvements and advances, the research's results help to progress RF power amplifier design. The suggested PA's potential importance and usefulness in real-world scenarios are highlighted by its proven reliability, efficiency, and compliance with wireless communication standards. This study encourages creativity and progression in the area by providing a foundation for future developments in RF power amplifier design.

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#### **Authors Contributions**

The contribution of the authors was as follows: Author A's contribution to this study was the concept, technical implementation, and correspondence. The methodology to conduct this research work was proposed by Author B. Data collection and supervision were performed by Author C. Author D facilitated the data compilation and validation. Author E's contribution was project administration, and paper writing.

#### **Conflict of Interest**

The authors declare no conflict of interest and confirm that this work is original and not plagiarized from any other source, i.e., electronic or print media. The information obtained from all of the sources is properly recognized and cited below.

#### **Data Availability Statement**

The testing data is available in this paper.

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